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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/290,342	VORBACH, MARTIN	
	Examin r	Art Unit	
	Stacy A Whitmore	2812	

-- Th MAILING DATE of this c mmunication app ars on the cov r she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-86* is/are pending in the application.

4a) Of the above claim(s) *69-78 and 81* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20,29-31,35,36,38,50-58,60-64,66,68,79,80 and 82-86* is/are rejected.

7)☒ Claim(s) *21-28,32-34,37,49,59,65 and 67* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/544,435* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claimed 63 and 66 are newly rejected, and therefore this office action is made non-final. Claim 80 was inadvertently indicated as allowable as the rejection has been maintained as cited for claim 80.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 57, and 60-61 are rejected under 35 U.S.C. 102(b) as being anticipated by Saleeba, "A self contained dynamically reconfigurable processor".

3. As for claim 57, Saleeba taught the invention as claimed, including a data processor comprising:

cells arranged in a multidimensional pattern [pg. 60-61, section 2, pg. 62 - fig. 2];

a first compiler for individually accessing and individually configuring at least some of the cells [pg. 60, section 2, first paragraph; pg. 61, fig. 1 and description], the first compiler selectively grouping the at least some of the cells with neighboring cells into functional units to perform a first function [pg. 60, section 2, first and third paragraphs; pg. 61, fig. 1 and description; pg. 64, section 6, third paragraph], the first compiler further selectively regrouping selected ones of the at least some of the cells into different functional units to perform a second function different than the first function while simultaneously others of the at least some of the cells process data [pg. 60, section 2, first and third paragraphs; pg. 61, fig. 1 and description; pg. 64, section 6, third paragraph: The second function is performed while simultaneously others of the at

least some of the cells process data because the partial reconfiguration is done at runtime, which is during processing].

4. As for claim 60, Saleeba further disclosed, the first compiler selectively regroups the selected one of the at least some of the cells by transmitting configuration data to at least one of the at least some of the cells, the at least one of the at least some of the cells reconfiguring to logically coupled to another of the cells as a function of the configuration data [pg. 60, section 2, first and third paragraphs; pg. 61, fig. 1 and description; pg. 64, section 6, third paragraph].

5. As for claim 61, Saleeba further disclosed second cells arranged in a second multi-dimensional pattern coupled in cascade with the cells [fig.'s 1 and 2].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 62-63, 64, 66, and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saleeba, M., "A self contained dynamically reconfigurable processor".

7. As for claims 62-63, (New) Saleeba taught the invention as claimed, including a data processor, comprising:

cells arranged in a multi-dimensional pattern [pg. 60-61, section 2, pg. 62 - fig. 2], at least one of the cells being selectively coupled to a first one of the cells to form a first functional unit at a first time [pg. 60, section 2, first and third paragraphs; pg. 61, fig. 1 and description; pg. 64, section 6, third paragraph], the first functional unit performing a first function [pg. 60, section 2, first and third paragraphs; pg. 61, fig. 1 and description; pg. 64, section 6, third paragraph], the at least one of the cells capable of being regrouped with a second one of the cells to form a second functional unit at a second time different from the first time [pg. 60, section 2, first and third paragraphs; pg. 61, fig. 1 and description; pg. 64, section 6, third paragraph], the second functional unit performing a second function different from the first function, the at least one of the cells regrouping as a function of reconfiguration data [pg. 64, section 6, third paragraph];

Saleeba further disclosed the use of state machines with regard to reconfigurable logic and determining program flow as a function of state information [pg. 64, first full paragraph].

Saleeba did not specifically disclose a first compiler receiving state information regarding the state of the first functional unit and transmitting reconfiguration data to the at least one of the cells as a function of the received state information.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Saleeba's state machine to inform the compiler of the state of configured functional units because the state machine would provide the necessary information for reconfiguration during runtime within Saleeba's system, which would improve performance of Saleeba's system.

8. As for claim 64, Saleeba further disclosed wherein selected ones of the at least one of the cells reconfigure to perform the respective second function while

simultaneously others of the at least some of the cells process data [pg. 61, fig. 1 and description of fig. 1, dynamic reconfigurability; and pg 62].

9. As for claim 68, Saleeba further disclosed second cells arranged in a second multi-dimensional pattern coupled in cascade with the cells [fig.'s 1 and 2].

10. As for claim 66, Saleeba further disclosed a segmented bus selectively coupling each of the cells to others of the cells [fig. 2, upper left hand section showing the segmented bus coupling the cells].

11. Claims 15-20, 29-31, 35-36, 38-48, 50-56, 79-80, and 82-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt (US Patent 5,410,723) in view of Saleeba, M., "A self contained dynamically reconfigurable processor".

12. As for claim 15, Schmidt taught the invention substantially as claimed, including a massively parallel data processing apparatus comprising:

a plurality of computing cells arranged in a multidimensional matrix, the plurality of computing cells capable of simultaneously manipulating a plurality of data [fig. 1; col. 3, lines 53-57; col. 4, lines 44-59], each of the plurality of computing cells including:

an input interface for receiving a plurality of input signals [fig. 2, handshake port and/or program memory]; a plurality of logic members, at least one of the pluralities of logic members coupled to the input interface [fig. 2, MAC, ALU];

at least one coupling unit selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals to arithmetic-logically configure the computing cell prior to processing the input signals, wherein coupled logic members perform at least one select arithmetic-logic operation on the input signals to process the input signals, the at least one select arithmetic-logic operation being dependent on the at least one of the plurality of configuration signals [col. 4, lines 44-68],

a register unit selectively storing a portion of the processed input signals [fig. 2, register rf; col. 5, lines 24-28], and

an output interface for transmitting the processed input signals [fig. 2, handshake ports; and col. 5, line 65 – col. 6, line 18],

wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells [fig. 2, handshake ports; and col. 5, line 65 – col. 6, line 18]; and

a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells [col. 4, lines 30-52].

Schmidt did not specifically disclose arithmetic-logically configuring the computing cell prior to processing the input signals.

Saleeba disclosed arithmetic-logically configuring the computing cell prior to processing the input signals [pg. 60-61, section 2,"compiler configurations"].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because arithmetic-logically configuring the computing cell prior to processing the input signals would have improved Schmidt's system by optimizing computing cells more efficiently which would improve performance of Schmidt's data processing apparatus [see Saleeba, pg. 61, last paragraph].

13. As for claim 16, Schmidt in view of Saleeba taught the invention substantially as claimed, including the data processing apparatus as cited in the rejection of claim 15.

Schmidt in view of Saleeba did not specifically disclose the coupling unit includes a multiplexer.

"Official Notice" is taken that both the concepts and advantages of the use of multiplexers as switching devices is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a multiplexer in the coupling unit in order to provide a switching device for the reconfiguring of the computing cells. Examiner cites Steenstra et al. (US Patent 5,649,179) [fig. 2; col. 2 ,lines 31-50; fig. 2] in support of the examiners position as requested by applicant.

14. As for claims17 and 18, and 79, 82, and 83, Schmidt further disclosed a plurality of lines for selectively coupling at least one of the plurality of computing cells to another of the plurality of computing cells to an adjacent and a non adjacent one of the plurality of cells, and a dataflow processor; each cell includes a cell configuration memory adapted to store at least one of a plurality of configuration signals; and wherein the cell configuration memory is dedicated to configuration information [fig. 1, fig. 2 (program memory); col. 5, and col. 6].

15. As for claim 19, Schmidt further disclosed a synchronization circuit [col. 4].

16. As for claim 20, Schmidt further disclosed wherein the synchronization circuit includes at least one of the plurality of computing cells [col. 8, lines 12-34].

17. As for claims 29-31, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including the massively parallel data processing apparatus as cited in the rejection of claim 15.

Schmidt further disclosed the external connection of the array processors with data transfer outside the array processor [col. 4, lines 37-50].

Schmidt did not specifically disclose the computing cells couple to an external memory device, a peripheral device, or another massively parallel data processing apparatus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to couple the computing cells to external devices such as memory, peripheral, of other processing devices in order to operate the data processing apparatus with other devices which are useful for storage of processed data, display of data, printing of data processing results of the combined computational power of connecting plural processor together.

18. As for claim 35, (Amended) Schmidt taught the inventions substantially as claimed, including a massively parallel data processing apparatus, comprising:

a plurality of computing cells arranged in a multidimensional matrix [fig. 1; col. 3, lines 53-57; col. 4, lines 30-59], each of the plurality of computing cells being arithmetic-logically configurable and reconfigurable [col. 4, lines 30-68], each of the plurality of computing cells capable of processing a first plurality of data words simultaneously with the processing of a second plurality of data words by others of the plurality of computing cells [col. 4, lines 30-68; and col. 5, lines 54-58], wherein each of the plurality of computing cells is arithmetic-logically configured by a first configuration signal to perform a first select arithmetic-logic operation [col. 4, lines 30-68; col. 5, lines 36-42],; and a plurality of buses, wherein each of the plurality of computing cells are connectable to at least one of the plurality of computing cells using at least one of the plurality of buses [].

Schmidt further disclosed the programmability of the computing cells [col. 1, lines54-57; and col. 4, lines 30-50].

Schmidt did not specifically disclose wherein each of the plurality of computing cells is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation.

Saleeba disclosed wherein each of the plurality of computing cells is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation [pg. 61, fig. 1 and description of fig. 1, dynamic reconfigurability; and pg 62].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because adding Saleeba's reconfigurability of the computing cells with a second configuration signal different from the first configuration signal would have improved Schmidt's system by efficiently reconfiguring the operation of the computing cells which would improve the operation of Schmidt's data processing apparatus [see Saleeba, pg. 61, last paragraph; pg. 62, last full paragraph].

19. As for claim 36, Schmidt further disclosed each of the plurality of computing cells maintaining a first configuration for a first period of time [col. 5, lines 35-42, and 54-58].

20. As for claim 38, Schmidt further disclosed at least one memory coupled to the processing apparatus for storing at least one of multiple data and processing results [col. 6, lines 6-20].

21. As for claim 39-41, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including a data processing apparatus as cited in the rejection of claims 35-36, and further disclosed an interface for transferring data externally [col. 6, lines 6-20].

Schmidt in view of Saleeba did not specifically disclose an external computer and memory device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Schmidt's interface for transferring data externally with external computer, other massively parallel data processing devices, a peripheral device or memory in order to interface Schmidt's processing apparatus with devices which are normally used with computer processing system such as memory and other computers for the sharing of data and further processing of data.

22. As for claim 42, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including the data processing apparatus as cited in the rejections of claims 35-36 as cited above, and Saleeba further disclosed a compiler capable of reconfiguring each cell independently without impairing other cells in their operation [pg. 61, fig. 1 and description of fig. 1, dynamic reconfigurability; and pg 62].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because dynamic configuration of some cells without impairing the operation of other cells would have improved the overall efficiency of Schmidt's system [see Saleeba, pg. 62].

23. As for claim 43, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including the data processing apparatus as cited in the rejections of claims 35-36, and 42 as cited above, and Saleeba further disclosed a memory coupled to the compiler, for storing first and second configuration signals [pg. 64, fig. 3 – RAM, pg. 68, section 7.2].

24. As for claim 44, Saleeba further disclosed wherein the compiler manages a plurality of configuration programs [pg. 61, fig. 1 and description].

25. As for claim 45, Schmidt further disclosed a synchronization circuit providing a plurality of synchronization signals for synchronizing the configuration of the at least some of the plurality of computing cells [col. 4, lines 11-27; col. 8, lines 12-18].

26. As for claim 46, Schmidt further disclosed at least one of the computing cells provides status information to the synchronization circuit [col. 8, lines 12-18].

27. As for claim 47 (Amended) Schmidt disclosed the invention substantially as claimed, including a massively parallel data processing apparatus, comprising:

a programmable logic device, the programmable logic device including a plurality of logic elements arranged in a multidimensional matrix [fig. 1; col. 3, lines 53-57; col. 4, lines 30-59], each of the plurality of logic elements being arithmetic-logically configurable [col. 4, lines 30-68], each of the plurality of logic elements capable of processing a first plurality of binary signals simultaneously with the processing of a second plurality of binary signals by others of the plurality of logic units [col. 4, lines 30-68], wherein each of the plurality of logic elements is arithmetic-logically configured to perform a first select arithmetic-logic operation by a first configuration signal [col. 4, lines 30-68; col. 5, lines 36-42],

the programmable logic device further comprising a plurality of buses, wherein each of the plurality of logic elements are connectable to at least one of the plurality of logic elements using at least one of the plurality of buses [fig. 1, fig. 2, col. 4, lines 30-50]; and at least one memory device coupled to the programmable logic device for storing at least one of i) multiple data to be processed by the programmable logic device, and ii) processing results of the programmable logic device [col. 4, lines 30-50; and col. 6, lines 6-35].

Schmidt further disclosed the programmability of the computing cells [col. 1, lines54-57; and col. 4, lines 30-50].

Schmidt did not specifically disclose and wherein each of the plurality of logic elements is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation

by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation.

Saleeba disclosed wherein each of the plurality of computing cells is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation pg. 61, fig. 1 and description of fig. 1, dynamic reconfigurability; and pg 62].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because adding Saleeba's reconfigurability of the computing cells with a second configuration signal different from the first configuration signal would have improved Schmidt's system by efficiently reconfiguring the operation of the computing cells which would improve the operation of Schmidt's data processing apparatus [see Saleeba, pg. 61, last paragraph; pg. 62, last full paragraph].

28. As for claim 48, Schmidt further disclosed each of the plurality of computing cells maintaining a first configuration for a first period of time [col. 5, lines 35-42, and 54-58].

29. As for claims 50-51, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including the massively parallel data processing apparatus as cited in the rejection of claim 47.

Schmidt further disclosed the external connection of the array processors with data transfer outside the array processor and an external interface [col. 4, lines 37-50; fig. 1 bus switch].

Schmidt did not specifically disclose a peripheral interface to a peripheral device, or optimized to couple to another massively parallel data processing apparatus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an interface optimized for coupling to peripheral devices or other processing devices in order to operate the data processing apparatus with other devices which are useful for storage of processed data, display of data, printing of data processing results of the combined computational power of connecting plural processor together.

30. As for claim 52, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including the data processing apparatus as cited in the rejections of claims 35-36 as cited above, and Saleeba further disclosed a compiler capable of reconfiguring each cell independently without impairing other cells in their operation [pg. 61, fig. 1 and description of fig. 1, dynamic reconfigurability; and pg 62].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because dynamic configuration of some cells without impairing the operation of other cells would have improved the overall efficiency of Schmidt's system [see Saleeba, pg. 62].

31. As for claim 53, Schmidt in view of Saleeba disclosed the invention substantially as claimed, including the data processing apparatus as cited in the rejections of claims 35-36, and 4243, and 47 as cited above, and Saleeba further disclosed a memory coupled to the compiler, for storing first and second configuration signals [pg. 64, fig. 3 – RAM, pg. 68, section 7.2].

32. As for claim 54, Saleeba further disclosed wherein the compiler manages a plurality of configuration programs [pg. 61, fig. 1 and description].

33. As for claim 55, Schmidt further disclosed a synchronization circuit providing a plurality of synchronization signals for synchronizing the configuration of the at least some of the plurality of computing cells [col. 4, lines 11-27; col. 8, lines 12-18].

34. As for claim 56, Schmidt further disclosed at least one of the computing cells provides status information to the synchronization circuit [col. 8, lines 12-18].

35. As for claims 84 and 85, Schmidt further disclosed a cell configuration memory [fig.'s 1, 2; and col. 5], and further computing cells coupled together in accordance with a first set of configuration words as cited in the rejection of claim 35..

Schmidt did not specifically teach a second set of words to reconfigure the cells.

Saleeba disclosed a second set of words to reconfigure the cells [pgs. 60-62 and as cited in the rejection of claim 35].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because reconfiguring the cells with a second word would provide for runtime reconfigurability thereby enhancing performance of Schmidt's system [see Saleeba, pg. 62].

36. As for claim 86, (New) Schmidt taught the inventions substantially as claimed, including a massively parallel data processing apparatus comprising: a plurality of computing cells arranged in a multidimensional matrix [fig. 1; col. 3, lines 53-57; col. 4, lines 44-59], the plurality of computing cells capable of simultaneously manipulating a plurality of data [fig. 1; col. 3, lines 53-57; col. 4, lines 44-59], each of the plurality of computing cells including:
an input interface for receiving a plurality of input signals [fig. 2, handshake port and/or program memory], a plurality of logic members, at least one of the plurality of logic members coupled to the input interface [fig. 2, MAC, ALU], at least one coupling unit

selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals [col. 4, lines 44-68], a cell configuration memory adapted to store the at least one of the plurality of configuration signals [fig. 2, program memory; col. 5, lines 36-42], a register unit selectively storing a portion of the processed input signals [fig. 2, register rf; col. 5, lines 24-28], and an output interface for transmitting the processed input signals [fig. 2, handshake ports; and col. 5, line 65 – col. 6, lines 18], wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells [fig. 2, handshake ports; and col. 5, line 65 – col. 6, lines 18]; and a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells [col. 4, lines 30-52].

Schmidt further disclosed that the computing cells are programmable [col. 1, lines 54-57; and col. 4, lines 30-50].

Schmidt did not specifically disclose that the computing cells are reconfigurable.

Saleeba disclosed arithmetic-logically reconfiguring the at least some of the plurality of computing cells [pg. 61, fig 1 and description of 1, dynamic reconfigurability; and pg. 62].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because adding Saleeba's arithmetic-logically reconfiguring the at least some of the plurality of computing cells to Schmidt's system would have improved Schmidt's system by efficiently reconfiguring the operation of the computing cells which would improve the operation of Schmidt's data processing apparatus [see Saleeba, pg. 61, last paragraph; pg. 62, last full paragraph].

37. As for claim 80, Schmidt further disclosed an interface for external connection and external data transfer [col. 6, and fig. 1, bus switch].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Schmidt's interface for use with an external computer, or memory device in order to perform computer processing operations such as data transfer and storage of processed data.

38. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saleeba, M., "A self contained dynamically reconfigurable processor" in view of Schmidt (US Patent 5,410,723).

39. As for claim 58, Saleeba taught the invention as claimed, including a data processor as cited in the rejection of claim 57, further including the compiler.

Saleeba did not specifically disclose state information from at least one cell in each functional unit, regrouping the cells based on the state information.

Schmidt disclosed state information from the cells [abstract, col.'s 5-6].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Saleeba and Schmidt because adding Schmidt's state information to Saleeba's system would have improved Saleeba's system by allowing for Saleeba's processing system to indicate the data flow status to the compiler which would improve program flow.

40. Claims 21-28, 32-34, 37, 49, 59, 65, and 67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

41. Applicant's arguments with respect to claims 15-68, and 79-80, 82-86, filed July 18, 2003, have been fully considered but they are not persuasive.

Applicant argues in substance:

Section I. With respect to claims 57, 60, and 61, Saleeba does not disclose the compiler can individually access or individually configure cells of the system.

Section II. With respect to claims 62, 64, and 68, Saleeba does not teach or suggest a compiler which receives state information regarding a first functional unit and transmits reconfiguration data to at least one of the cells as a function thereof. Applicant also argues hindsight reconstruction.

Section III. Applicant argues with respect to claims 15-20, 29-31, 35-36, 38-48, 50-56, 79, and 82-86 the following:

A - With respect to claim 15, the combination of Schmidt in view of Saleeba does not teach or suggest arithmetically-logically configuring the computing cell prior to processing the input signals; that the combination of Schmidt in view of Saleeba is hindsight reconstruction; and that Schmidt is a wavefront processor which is not reconfigurable at run-time, thereby only being fixedly arranged array of processors.

B - With respect to claim 16, that a multiplexer to provide a switching device for the reconfiguring of the computing cells.

C - With respect to claims 17-20, 79, 82, and 83, the same arguments apply as to claim 15, and additionally with respect to claim 18, the combination of Schmidt and Saleeba does not teach non-adjacent cells may be coupled.

D - With respect to claims 29-31, applicant traverses the Official Notice and request a reference for the limitation of coupling computing cells to an external memory device, a peripheral device, or another massively parallel data processing apparatus.

E – With respect to claims 36, and 38-46, and claim 80 which also is rejected, applicant further argues that Saleeba did not disclose an external computer and memory device and request a reference.

F – With respect to claims 35 and 47, buses interconnecting the plurality of logic elements is not disclosed by the combination of Schmidt in view of Saleeba.

G – With respect to claims 48, 50-56, and 84-85, applicant further argues with respect to claims 50-51, Schmidt in view of Saleeba does not disclose the peripheral interface and request a reference.

Section IV.

With respect to claim 58, Schmidt nor Saleeba teaches or suggests the use of state information from a cell by a compiler. This is similar to the arguments presented in claims 62, 64, and 68 and has been addressed in the examiner's response to the arguments presented in claims 62, 64, and 68.

Examiner respectfully disagrees for the following reasons:

Section I. With respect to claims 57, 60, and 61, Saleeba does disclose the compiler can individually access or individually configure cells of the system. [See as cited in the prior rejection and further figure 1 with the explanation box referring to figure 1. Figure 1 shows that the multidimensional array of cells may be individually accessed and configured because the individual subroutines are individually accessed and configured as shown that only subroutine F was changed in the example during run-time.]

Section II. With respect to claims 62, 64, and 68, Saleeba does not teach or suggest a compiler which receives state information regarding a first functional unit and transmits reconfiguration data to at least one of the cells as a function thereof. Applicant also argues hindsight reconstruction.

First - In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was

within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Second – As cited in the rejection of claims 62, 64, and 68 above, and further explained.

Saleeba further disclosed the use of state machines with regard to reconfigurable logic [pg. 64, first full paragraph].

Saleeba did not specifically disclose a first compiler receiving state information regarding the state of the first functional unit and transmitting reconfiguration data to the at least one of the cells as a function of the received state information.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Saleeba's state machine to inform the compiler of the state of configured functional units because the state machine would provide the necessary information for reconfiguration during runtime within Saleeba's system, which would improve performance of Saleeba's system. **Further**, the Saleeba's compiler oriented reconfigurable system which is dynamically reconfigured at run-time would greatly benefit from the state machines in order to determine what cells are busy and/or free to reconfigure during processing, which would allow for reconfigurability of Saleeba's reconfigurable processor without just blindly sending information to computing cells in an non-optimized fashion. Saleeba's system would be improved by knowing which processing cells are free through state machine information.

Section III. Applicant argues with respect to claims 15-20, 29-31, 35-36, 38-48, 50-56, 79, and 82-86 the following:

A - With respect to claim 15, the combination of Schmidt in view of Saleeba **does teach or suggest** arithmetically-logically configuring the computing cell prior to processing the input signals ; that the combination of Schmidt in view of Saleeba is hindsight reconstruction; and that Schmidt is a wavefront processor which is not reconfigurable at run-time, thereby only being fixedly arranged array of processors.

First – Saleeba disclosed arithmetic-logically configuring the computing cell prior to processing the input signals [pg. 60-61, section 2,"compiler configurations"] as disclosed in the prior office action.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schmidt and Saleeba because arithmetic-logically configuring the computing cell prior to processing the input signals would have improved Schmidt's system by optimizing computing cells more efficiently which would improve performance of Schmidt's data processing apparatus [see Saleeba, pg. 61, last paragraph].

Furthermore, Schmidt suggests that the computing cells are configured via a programming bus, which although expressly stated, may include configuring the cells prior to processing input signals col. 4, lines 30-36]

Second – In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does

not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Third - Schmidt is reconfigurable at run-time, and not only being fixedly arranged array of processors [col. 4, lines 30-36, where Schmidt disclosed that the cells usually remain constant, or are seldom modified, which reads as configurable via the programming bus which includes run-time]. Furthermore, the argument Schmidt is a wavefront processor which is not reconfigurable at run-time, thereby only being fixedly arranged array of processors is not a claimed limitation, and therefore is rendered moot.

B - With respect to claim 16, that a multiplexer to provide a switching device for the reconfiguring of the computing cells. Examiner stated "Official Notice" is taken that both the concepts and advantages of the use of multiplexers as switching devices is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a multiplexer in the coupling unit in order to provide a switching device for the reconfiguring of the computing cells. Examiner cites Steenstra et al. (US Patent 5,649,179) [fig. 2; col. 2, lines 31-50; fig. 2] in support of the examiners position as requested by applicant.

C - With respect to claims 17-20, 79, 82, and 83, the same arguments apply as to claim 15, and additionally with respect to claim 18, the combination of Schmidt and Saleeba does not teach non-adjacent cells may be coupled. The combination of Schmidt in view of Saleeba does disclose non-adjacent cells my be coupled [see Saleeba pg. 61, fig. 1 – dynamically reconfigurable machine; see also Schmidt; fig. 1,

applicants claim language as applied to Schmidt does not exclude the coupling of elements distantly coupled together, therefore Schmidt also reads on the claim language]

D - With respect to claims 29-31, applicant traverses the Official Notice and request a reference applicant traverses the Official Notice and request a reference for the limitation of coupling computing cells to an external memory device, a peripheral device, or another massively parallel data processing apparatus.

Examiner made an obviousness statement with respect to the cited references suggestion of external devices, and clarifies the suggestion of connection to external devices such as peripheral devices [col. 4 lines 14-15, and 48-50]

Examiner stated in the prior rejection that Schmidt further disclosed the external connection of the array processors with data transfer outside the array processor [col. 4, lines 37-50].

Schmidt did not specifically disclose the computing cells couple to an external memory device, a peripheral device, or another massively parallel data processing apparatus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to couple the computing cells to external devices such as memory, peripheral, of other processing devices in order to operate the data processing apparatus with other devices which are useful for storage of processed data, display of data, printing of data processing results of the combined computational power of connecting plural processor together.

Examiner cites **Dolecek (US Patent 4,720,780)** [col. 5, lines 22-25, elements 10 and 16; col. 5, lines 51-52, fig. 1b element 30; figs. 2, 3, and 12 input and output interface; fig. and col. 6, lines 53-55] for support of the "Official Notice" taken with respect to claims 29-31.

E – With respect to claims 36, 38-46, and also claim **80**, applicant further argues that Saleeba did not disclose an external computer and memory device and request a reference. Examiner made an obviousness rejection with respect to claims 39-41:

Schmidt in view of Saleeba disclosed the invention substantially as claimed, including a data processing apparatus as cited in the rejection of claims 35-36, and further disclosed an interface for transferring data externally [col. 6, lines 6-20].

Schmidt in view of Saleeba did not specifically disclose an external computer and memory device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Schmidt's interface for transferring data externally with external computer, other massively parallel data processing devices, a peripheral device or memory in order to interface Schmidt's processing apparatus with devices which are normally used with computer processing system such as memory and other computers for the sharing of data and further processing of data.

Examiner cites **Dolecek (US Patent 4,720,780)** [col. 5, lines 22-25, elements 10 and 16; col. 5, lines 51-52, fig. 1b element 30; figs. 2, 3, and 12 input and output interface;

fig. and col. 6, lines 53-55] for support of the "Official Notice" taken with respect to claims 36, and 38-46.

F – With respect to claims 35 and 47, buses interconnecting the plurality of logic elements is not disclosed by the combination of Schmidt in view of Saleeba.

Buses interconnecting the plurality of logic elements is disclosed by Schmidt in view of Saleeba [see Schmidt, fig. 1, the buses between all the cells; see Saleeba, fig. 2, upper left hand of figure showing the buses between the processing elements].

G – With respect to claims 48, 50-56, and 84-85, applicant further argues with respect to claims 50-51, Schmidt in view of Saleeba does not disclose the peripheral interface and request a reference.

Examiner cites **Dolecek (US Patent 4,720,780)** [col. 5, lines 22-25, elements 10 and 16; col. 5, lines 51-52, fig. 1b element 30; figs. 2, 3, and 12 input and output interface; fig. and col. 6, lines 53-55] for support of the "Official Notice" taken with respect to claims 35 and 47.

Section IV.

With respect to claim 58, Schmidt nor Saleeba teaches or suggests the use of state information from a cell by a compiler. This is similar to the arguments presented in claims 62, 64, and 68 and has been addressed in the examiner's response to the arguments presented in claims 62, 64, and 68.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SW
October 22, 2003